VLSI Design
Sem 6

1 mark questions:

P-well is created on _____
p substrate
n substrate
p & n substrate
p- substrate

The isolated active areas are created by technique known as _____
Etched field-oxide isolation
Local Oxidation of Silicon
Etched field-oxide isolation or Local Oxidation of Silicon
Ion implantation

The parasitic capacitances found in MOSFET are _____
Oxide related capacitances
Inter electrode capacitance
Electrolytic capacitance
A, B and C

For complex gate design in CMOS, OR function needs to be implemented by _____ connection/s of MOS.

Series
Parallel
Both series and parallel
Combination of series and parallel

In CMOS logic circuit the p-MOS transistor acts as:
Pull down network
Pull up network
Load
Short to ground

Implementing the switches in Pass transistor logic circuit with single NMOS resistor results in a circuit with
Large area
Small area
Zero area
Infinite area

When one pass transistor is driven using another, threshold voltage
affects
does not affect
decreases
increases

In dynamic CMOS logic _____ is used.
two phase clock
three phase clock
one phase clock
four phase clock

Which one of the following is a storage element in SRAM?
capacitor
inductor
transistor
resistor

The problem of carrying propoagation delay was resolved by
4 bit adder
Parallel adder
Ripple carry adder
Carry look adder

2 marks questions:

For on-chip generation of a primary clock signal _____ circuit can be used
Ring oscillator
Colpitts Oscillator
LC oscillator
Hartley Oscillator

The subthreshold conduction current also sets a severe limitation against
reducing the threshold voltage
reducing the supply voltage
reducing the aspect ratio
reducing the device dimension

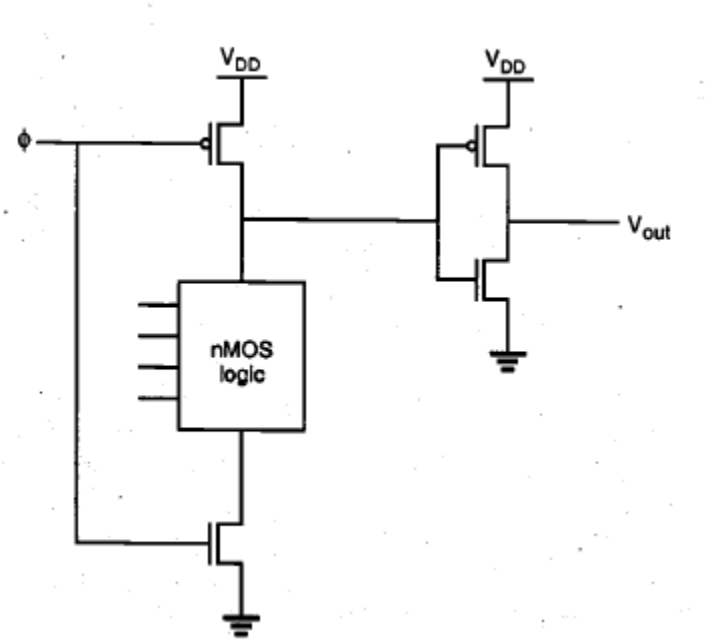
For a given memory structure there are 2^N rows and 2^M columns. The total number of memory cells are
N X M
2 (N X M)
2^N X 2^M
N X 2^M

Basic architecture of Zipper CMOS is identical to _____ with the exception of clock signals
NORA CMOS
Pass Transistor Logic
Transmission gate
Domino Logic

In CMOS inverter, transistor is a switch having _____
a) infinite on resistance
b) finite off resistance
c) buffer
d) infinite off resistance

In a CMOS inverter, when $\beta n = \beta p$, threshold voltage moves closer to
Zero
Infinity
Midpoint value
Supply voltage

Figure below shows



Pass transistor logic
CMOS transmission gate
DOMINO CMOS Logic
C2MOS logic

Crosstalk can be reduced by
Differential Signaling
Shielding in the layout
Both differential signaling and shielding in the layout
Reducing Voltages

Carry generator in full adder has expression
G = AB
G = A+B
G = A-B
G = A\B

The carry propagation delay in 4-bit full-adder circuits _____
Is cumulative for each stage and limits the speed at which arithmetic operations are performed
Is normally not a consideration because the delays are usually in the nanosecond range
Decreases in direct ratio to the total number of full-adder stages
Increases in direct ratio to the total number of full-adder stages, but is not a factor in limiting the speed of arithmetic operations

Sense amplifiers are essential to the proper operation of

DRAM
SRAM
TRAM
RRAM

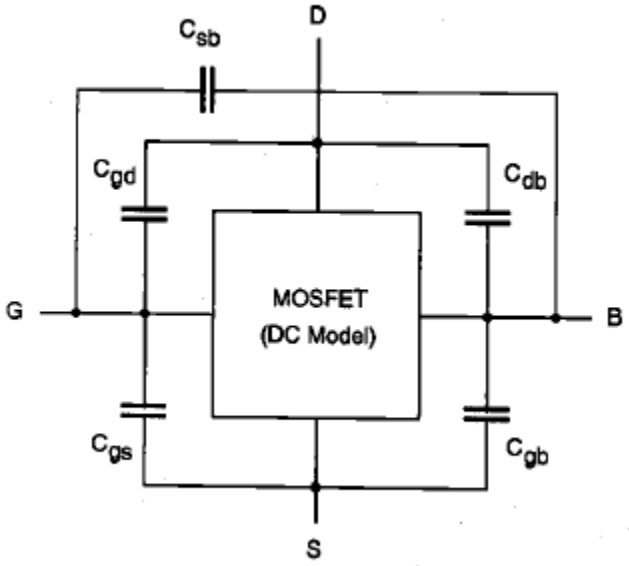
A form of dynamic logic that results in cascaded gates is termed as
TTL logic
PTL logic
DOMINO CMOS logic
CMOS logic

When both nMOS and pMOS transistors of CMOS logic design are in OFF condition, the output is:
1 or Vdd or HIGH state
0 or ground or LOW state
High impedance or floating(Z)
Cannot be determined

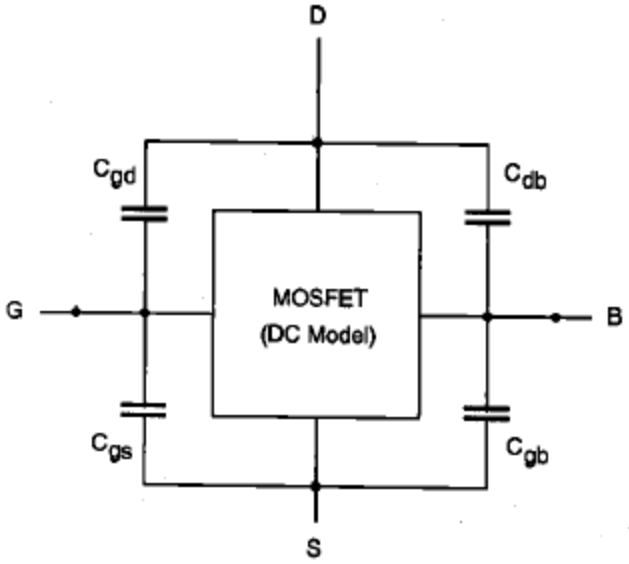
The total load capacitance is calculated as the sum of _____
Drain capacitance in series with input capacitance
Drain capacitance + interconnect capacitance +input capacitance
Drain capacitance + interconnect capacitance – input capacitance
Drain capacitance in parallel with input capacitance

When MOSFET is operating in saturation region, the gate to source capacitance is?
1/2*Cox*W*L
2/3*Cox*W*L
Cox*W*L
1/3*Cox*W*L

The proper DC model of MOSFET with capacitances is?

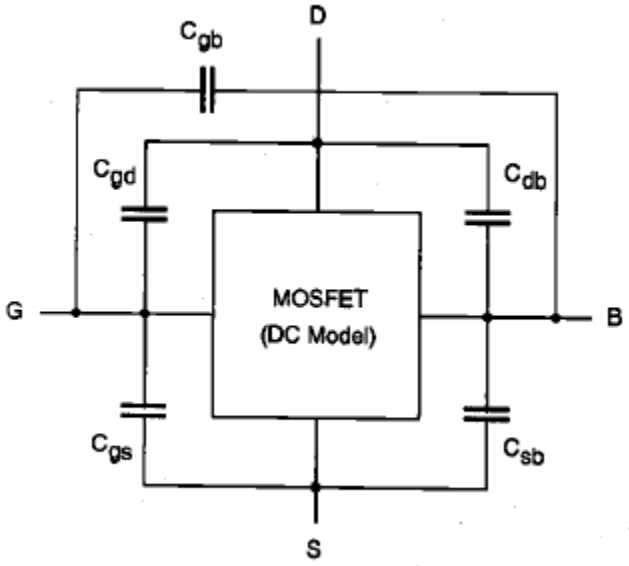

D
C_{sb}
C_{gd}
C_{db}
G
MOSFET
(DC Model)
B
C_{gs}
C_{gb}
S

a.

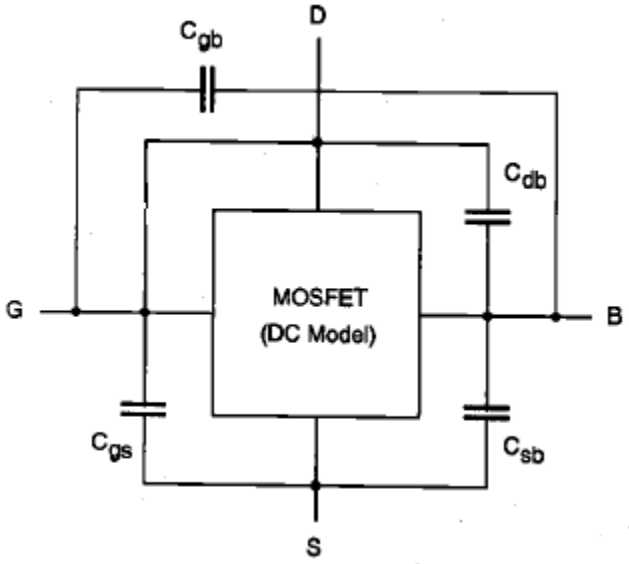

D
C_{gd}
C_{db}
G
MOSFET
(DC Model)
B
C_{gs}
C_{gb}
S

b.

c.



d.



Minimum n-well width should be _____ micro meter.

2

3

4

6

Which layer is used for power and signal lines?

metal

polysilicon

n-diffusion
p-diffusion

P-well doping concentration and depth will affect the _____
threshold voltage
Vss
Vdd
Vgs

_____ is sputtered on the whole wafer.
silicon
calcium
potassium
aluminium